Design and Analysis of Capacitor Assisted Extended Boost Quasi ZSI

Rini Paul, Binitha Joseph Mampilly

Abstract—The quasi Z-source inverter is a very attractive topology because of its unique capability of voltage boost and buck functions in a single stage. But its voltage boost property could be a limiting feature in some applications where very high input voltage gain is required. This input voltage gain could be extended by the implementation of the capacitor assisted quasi-impedance network. This paper discusses a capacitor assisted quasi-Z-source inverter. Steady state analysis and design of the topology operating under continuous conduction mode is presented. Performances were analyzed in the steady state and validated using simulation and hardware results.

Index Terms— Extended boost, Quasi Z-source inverters, Capacitor assisted qZSI, Maximum boost control, Impedance network design, Operationg principle, Hardware results.

1 INTRODUCTION

THE Z-source inverter (ZSI) was introduced in order to overcome limitations of conventional voltage-source (Vsource) and current-source (I-source) converters [1]. The ZSI provides special features which cannot be noticed in the trad tional inverter; they are as follows.

- The ZSI is a self-boost converter for dc-to-ac power conversion and a desired ac voltage can be obtained, which is greater than the source line voltages.
- A short circuit across any phase leg is allowed, so that the dead time is not a necessary attribute.
- Second-order filters are provided, which are more effective to suppress voltage ripples than the capacitor used in the traditional PWM inverter.
- The in-rush current and harmonics in the current can be reduced due to the inductor.

The traditional Z-source inverter structure, which consists of two inductors and two capacitors connected in X shape connects the inverter to the dc voltage source, which may be a battery, a diode rectifier, or a fuel cell. The Z source network is utilized to boost the DC link voltage to a desired level which could be equal or greater than the DC voltage. A voltage boost is necessary when voltage sag occurs in the DC side or the load needs a higher voltage level than the voltage level provided by the DC side.

However, unlike VSI, the original ZSI does not share the ground point of dc source with the converter and also the current drawn from the source will be discontinuous, and these would be a disadvantage in some applications; it may be required to have a decoupling capacitor bank at the front end to avoid current discontinuity and to protect the energy source.

2 QUASI Z SOURCE INVERTER

The traditional ZSI has been modified, as shown in Fig. 1(a) and (b), where now a modified impedance network is placed at the bottom or top arm of the inverter [2]. These topologies are named as quasi-ZSIs (qZSIs). The advantage of these topologies is that the voltage stress on the capacitor is much lower, as compared to that of the traditional ZSI. Need of high

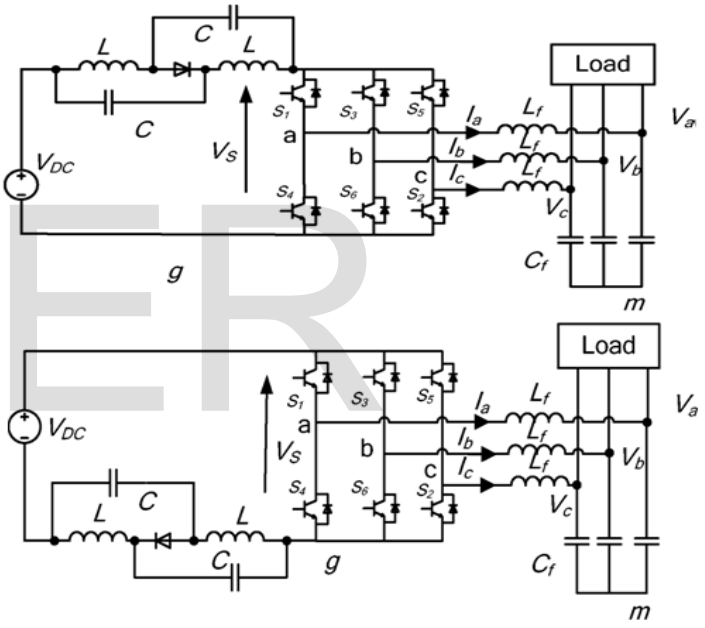

Fig. 1. Discontinuous-current qZSI with shared ground

415V three-phase systems.In the case of fuel and solar cells, although it is possible to increase the number of cells to increase the voltage, there are other influencing factors that need to be taken into account. Sometimes the available number of cells is limited or env ronmental factors could come into play due to shading of light on some cells that could result in poor overall energy catchments. In the case of fuel cells, some manufactures produce them as lower voltage system to achieve a faster response [3]. Such factors could demand power converters with larger boost ratio. This cannot be realized with a single qZSI or traditional ZSI.

3 CAPACITOR ASSISTED EXTENDED BOOST QUASI Z SOURCE INVERTER.

A discontinuous-current qZSI inverter is used as the basic topology to extend the boosting capability. The topology is ca-

pacitor-assisted extended boost QZSI (CAEBQZSI). Topology can be modulated using the modulation methods proposed for the original ZSI. The advantage of expandability was not possible with the original ZSI, i.e., if one needs to increase the boosting rage, another stage can be cascaded at the front end without increasing the number of active switches [4]. The only additions for each added new stage would be one inductor, two capacitors, and one diode for the capacitor-assisted case. For added new stage, the boost factor would change to $1/(1-3D_S)$ compared to $1/(1-2D_S)$ in the traditional qZSI, where D_S = shoot through duty ratio. For second extension boost factor is changed to $1/(1-4D_S)$.

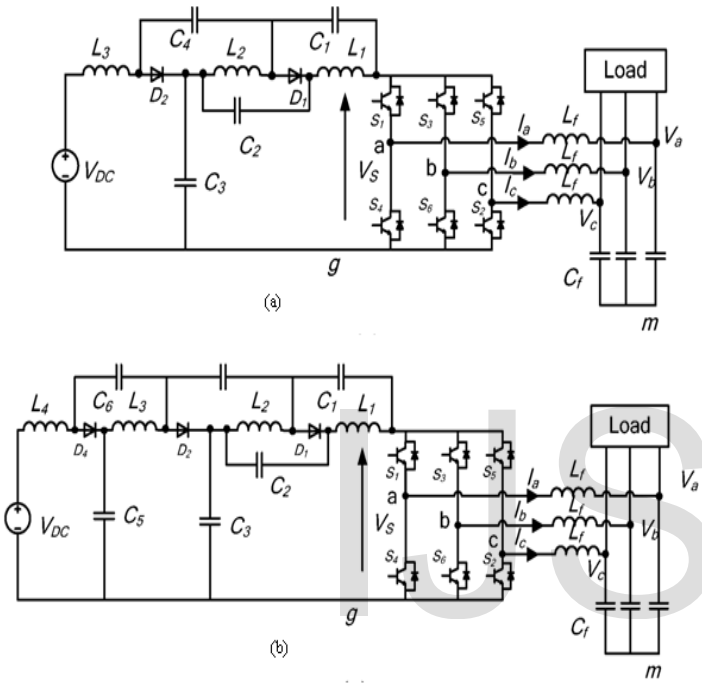

Fig. 2. CAEBQZSI (a) First extension. (b) Second extension.

Fig 2. (a) Shows the voltage fed capacitor assisted extended boost quasi Z source inverter continuous current with first extension. It can be extended to have a very high boost by cascading more stage as shown in Fig 2. (b). Similar to the traditional QZSI, the converter's operating states are simplified into shoot through and non shoottthrough states. This new extended topology comprises an additional inductor, a diode, and two capacitors to the QZSI. The operating principle of this additional impedance network is similar to that found in the cascaded boost and Luo converters. The added impedance network provides the boosting function without disturbing the operation inverter.

3.1 Operating Principle

The inverter's operating states are simplified into non shoot-through and shoot-through states. The inverter bridge, viewed from the DC side is equivalent to a current source. The boosted input dc voltage is available as DC link voltage input to the inverter, which makes the QZSI behave similar to a VSI. Fig 3 (a) shows the equivalent circuit in Active mode and (b) shows the equivalent circuit in Shoot through Mode. During active mode, switching pattern for the QZSI is similar to that of a VSI and here diodes D1 and D2 are conducting. The inductors discharge when the capacitors get charged. In the shoot through mode switches of the same phase in the inverter bridge are switched on simultaneously for a very short duration. The source however does not get short circuited when attempted to do so because of the presence LC network, while boosting the output voltage. Here both the diodes D1 and D2 are in blocking state. The inductors get charged and energy is transferred from the source to inductors or the capacitor to inductors while capacitors are getting discharged. The DC link voltage during the shoot through states, is boosted by a boost factor, whose value depends on the shoot through duty ratio for a given modulation index.

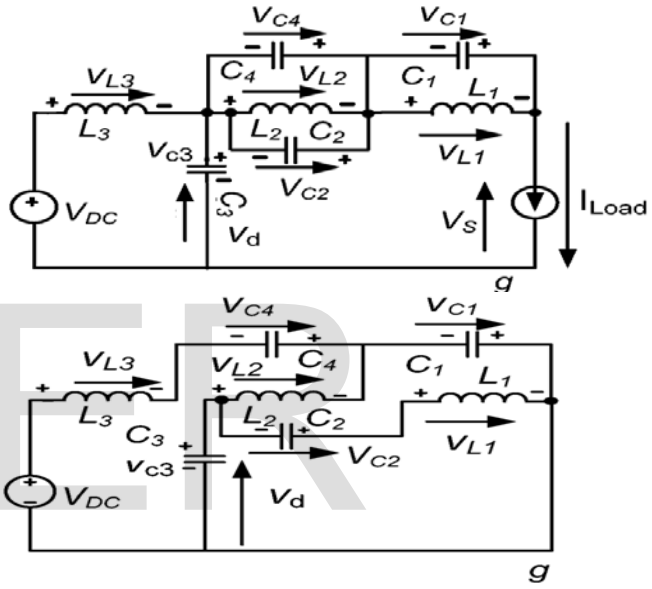

Fig.3 Simplified diagram of the capacitor-assisted extended-boost continuous current qZSI. (a) Non shoot-through state. (b) Shoot through state.

3.2 Circuit analysis

Assuming that during one switching cycle, T, the interval of the shoot through state is T_0; the interval of nonshoot- through states is T_1; thus one has $T = T_0 + T_1$ and the shoot-through duty ratio, $D_S = T_0 / T_1$. First, consider the interval of the non-shoot-through states, T_1. Then by applying KVL, the following steady-state relationships can be observed as

$V_{dc} + V_{L3} = V_{C3}$, $V_{C3} + V_{C2} + V_{C1} = V_S$ and
$V_{C3} + V_{C4} + V_{C1} = V_S$, $V_{C1} = V_{L1}$, $V_{C2} = V_{L2}$, $V_{C3} = V_d$, and
$V_{C2} = V_{C4}$.

During the interval of the shoot-through states, $T0$, similar relationships can be derived as

$V_{dc} + V_{L3} + V_{C4} + V_{C1} = 0$,
$V_{dc} + V_{L3} + V_{C4} - V_{L2} - V_{C3} = 0$,
$V_d + V_{L1} + V_{C2} = 0$,
$V_d + V_{L2} + V_{C1} = 0$ and $V_s = 0$.

Considering the fact that the average voltage across the inductors is zero, the following relationships can be derived:

$$V_{c3} = V_{c2} = V_{c4} = \frac{D_s}{1-2D_s} V_d = \frac{D_s}{1-3D_s} V_{dc} \quad (1)$$

$$V_{c3} = V_{c2} = V_{c4} = \frac{D_s}{1-2D_s} V_d = \frac{D_s}{1-3D_s} V_{dc} \quad (2)$$

Then from the aforementioned equations, the peak voltage across the inverter Vs can be obtained as follows:

$$V_s = \frac{1}{1-3D_s} V_{dc} = BV_{dc} \quad (3)$$

From the above equation the peak ac-output voltage V_x of a three phase inverter can be written as,

$$V_x = \frac{MV_s}{2} = \frac{MBV_{dc}}{2} \quad (4)$$

The average current of the inductors L_1, L_2 can be calculated by the system power rating P

$$I_{L1} = I_{L2} = I_{L3} = I_{in} = \frac{P}{V_{in}} \quad (5)$$

According to Kirchhoff's current law and we also can get that

$$I_{C1} = I_{C2} = I_{PN} - I_{L1} \quad (6)$$

The voltage across the capacitor is much smaller than conventional ZSI. Similarly it is possible to derive the boost factor for the second extension of the topology as $B = 1/[(1 - 4D_S)]$. To give a better representation of proposed topologies in relation to voltage boosting and applied voltage stress on the devices, Fig. 4 is plotted.

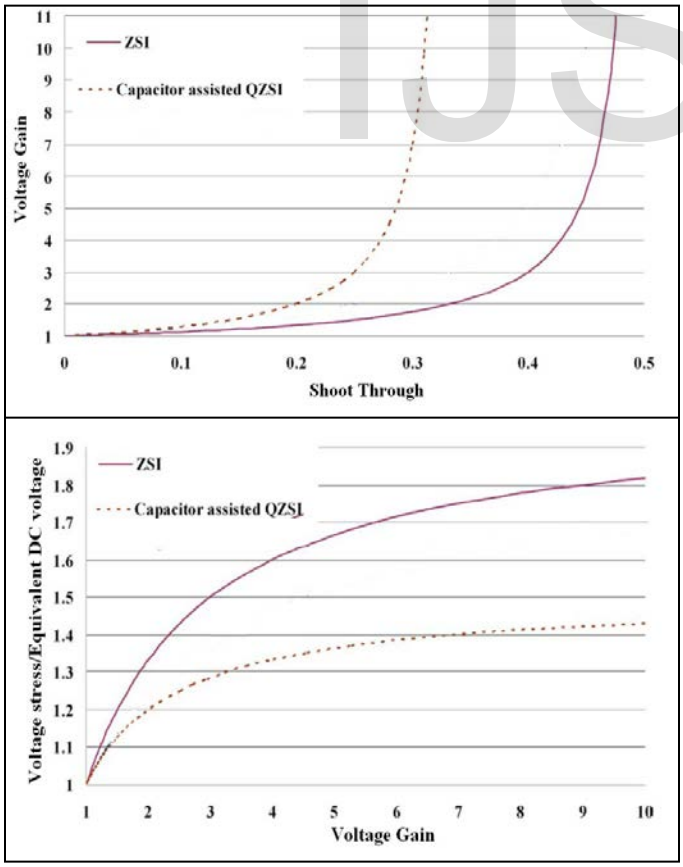

Fig 4. Voltage-boosting capability and voltage stress comparison ofdifferent topologies.

3.3 Inductor and Capacitor Design

In the PWM control strategy the frequency of the carrier fc is 10kHz and the shoot-through frequency fs as seen by the network is doubled to 20 kHz. When the system is operating in boost conversion mode, the potential maximum interval of the shoot-through T0, per switching cycle, can be calculated by,

$$T_{0\_max} = \frac{2-\sqrt{3}M_{min}}{fs}, \text{ for maximum boost control} \quad (7)$$

The inductors in the network will limit the current ripple through the devices during boost conversion mode. During shoot through mode, the inductor current increases linearly and the voltage across the inductor is equal to the voltage across the capacitor. The average current through the inductor is given by,

$$I_L = \frac{P}{Vdc} \quad (8)$$

where P is the total power and Vdc is the input voltage. Choosing an acceptable peak to peak current ripple, rc%, e.g. 15% in this application, the inductance can be calculated by

$$L_1 = L_2 = L_3 = \frac{V_L \Delta T}{\Delta I} \quad (9)$$

During shoot-through the capacitor charges the inductors and the current through the capacitor equals the current in the inductor. They absorb the current ripple and limit the voltage ripple on the inverter bridge so as to keep the output voltage sinusoidal. Assuming that the capacitance should be the same for each capacitor, the capacitance needed to limit the dc link voltage ripple by rv%, e.g. 0.17%, can be calculated by

$$C_1 = C_2 = C_3 = C_4 = \frac{2.I_{Cavg}.T_{0\_max}}{\Delta V_C} \quad (10)$$

3.4 PWM Control

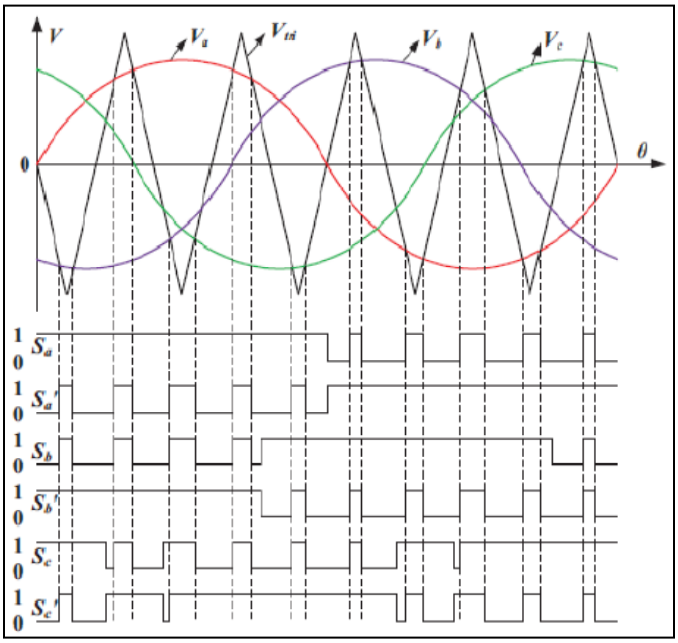

Fig. 5. Maximum boost control strategy

Reducing the voltage stress under a desired voltage gain becomes more important to control the quasi ZSI. Maximum boost control method [6] converts all traditional zero states to shoot-through while maintaining the six active states remain unchanged. This is obtained by comparing the maximum and the minimum curve of the sinusoidal reference with the triangular carrier. Whenever the maximum is lower than the triangular or the minimum is higher than the maximum and the minimum curve of the sinusoidal reference triangular, the inverter shoots through. Otherwise, it operates in the traditional PWM mode. By this control strategy the shoot-through duty cycle varies each cycle. The inverter gains maximum shoottthrough time which in turn gives the inverter higher boost factor, according to equation 3. Thus, with the same modulation index as in other control methods, we get higher voltage gain. Fig.5 shows the maximum boost control strategy.

4 Simulation Results

Simulation studies are performed on the open-loop configuration of the capacitor-assisted topology in MATLAB/ Simulink. Input voltage is kept constant at 100 V and a three-phase induction motor of 0.18kW, 415V and 1430rpm is used as the load. All dc-side capacitors are 1500 µF and inductors are 1 mH. In the non shoot through period the boosted DC voltage is inverted to AC. The components used in the simulation were as per the design. The input inductor is designed to limit current ripples. The capacitors absorb the current ripple and limit the voltage ripple on the inverter bridge so as to keep the output voltage sinusoidal. The capacitor assisted quasi z source inverter has two stages of control, one is DC side control and the other is ac voltage control. In the dc control the input voltage is boosted up. In the ac side control is similar to the conventional inverters i.e. dc voltage is inverter to ac.

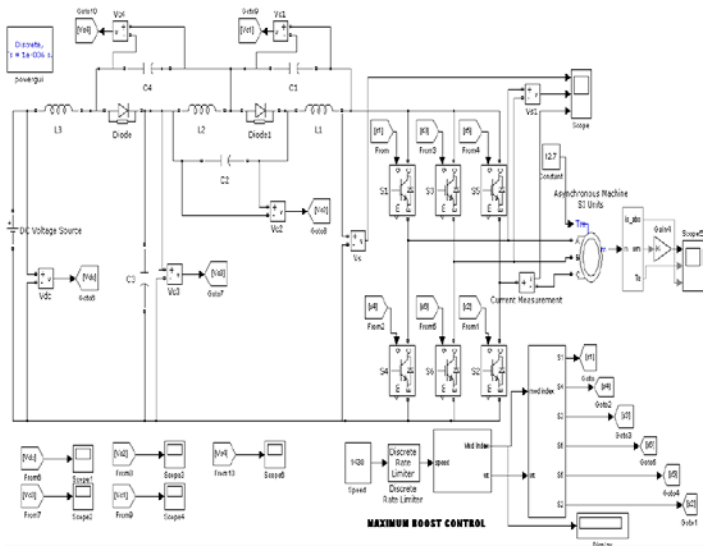

Fig 6. Simulation of the capacitor assisted topology in CCM

Figs. 7 and 8 show the simulation results, corresponding to capacitor-assisted topologies shown in Fig. 6 where they are operated with shoot-through value of 0.289 and modulation index of 0.859 to achieve a line-to-line output voltage of 415 V.

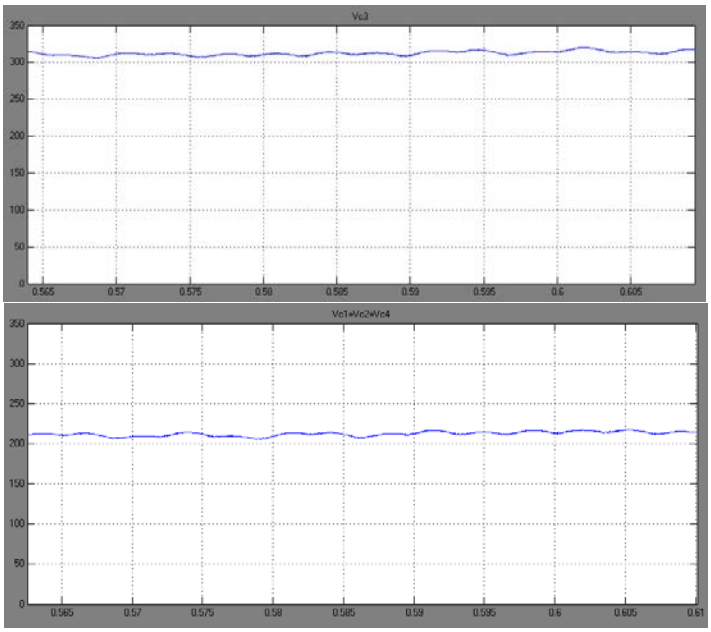

Fig 7. Stored capacitor voltages for boosting action

Topology produce a voltage boost of 760 V peak at the dc link in the case of continuous-current topology and equal voltage of 220 V across the capacitors *C*1, *C*2, and *C*4. Whereas, voltage across the capacitor *C*3 is 320 V. All simulation results comply with the equations derived in Section III and validates the operation of the topology.

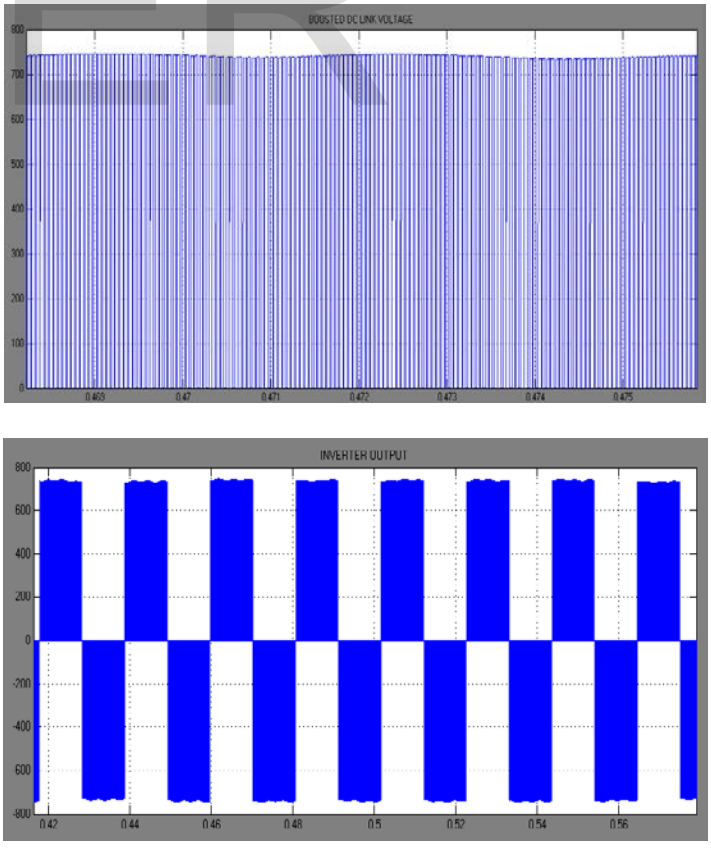

Fig 8. Boosted DC link voltage and the AC voltage output from the inverter.

5 HARDWARE RESULTS

The hardware set up for the analysisof capacitor assisted quasi Z-source inverters mainly contains the impedance network , inverter, dSPACE RTI1104 for generating firing pulses , driver circuit , the power circuit and the load. The prototype is implemented using MOSFET. The switching frequency is selected as 10 kHz and the components were designed for 0.18kW power output and the input supply is 30V DC. A three phase induction motor of 0.18kW, 415V, and 1430 rpm is connected as the load.. The results obtained with the hardware prototype of the capacitor assisted quasi z source inverter are shown below. Waveform shows that output voltage magnitude is greater than input voltage. Also the boosted DC link voltage is the sum of capacitor voltages V_{C3}, V_{C2} and V_{C4}.

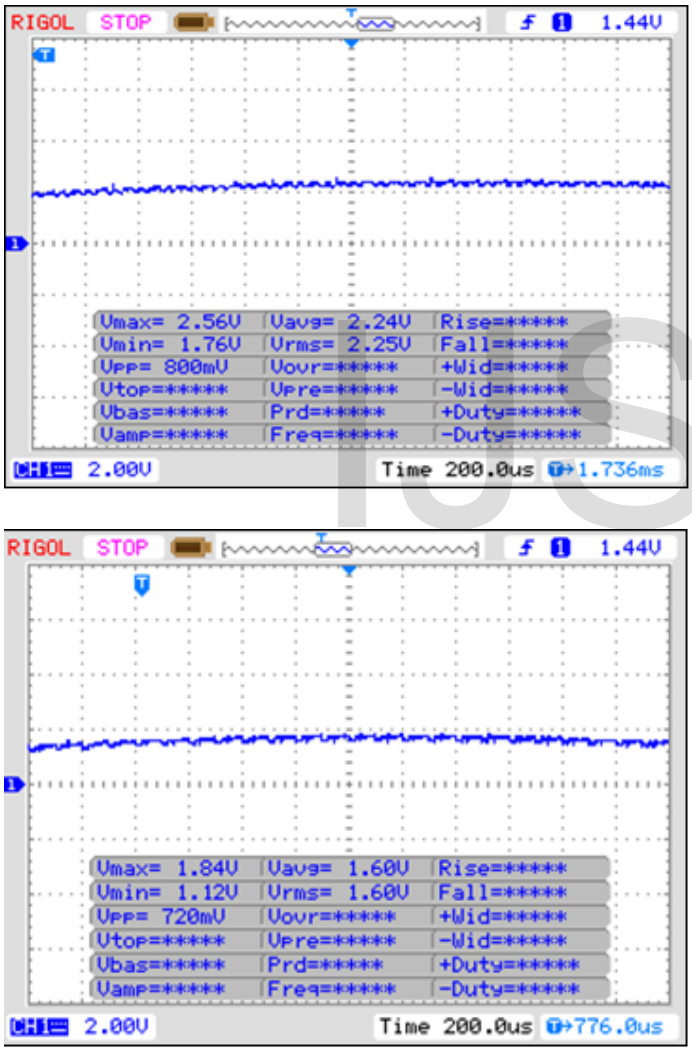

Fig 9 Stored capacitor voltages

Topology produces a voltage boost of 57 V peak at the dc link and equal voltage of 16 V across the capacitors C_1, C_2, and C_4. Whereas the voltage across the capacitor C_3 is 22 V. All simulation results comply with the equations derived and validates the operation of the topology.

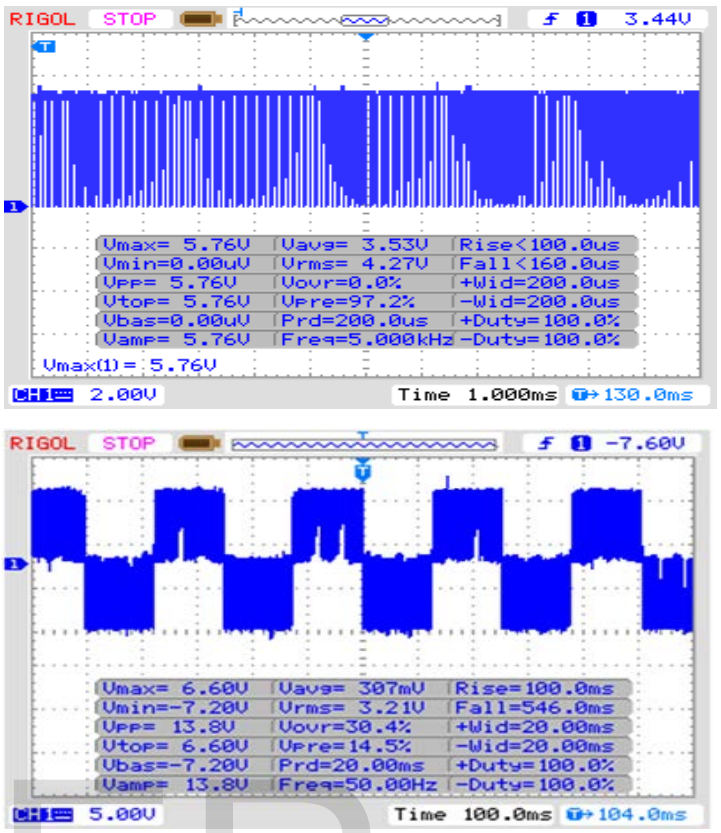

Fig 10 The boosted dc link voltage and the output voltage waveform

CONCLUSION

The power conversion circuit used here consists of a single stage with a qZSI, the power circuit and the controller were simple and can achieve a better efficiency. The capacitor assisted qZSI inherits all the advantages of the conventional qZSI and features its unique merits. It can realize boost power conversion in a single stage with a wide range of gain. Therefore the input DC voltage can be boosted to the required value and then used in various applications. The topology has the following merits.

1. The Z source capacitor voltage stress is reduced greatly to perform the same voltage boost, thus enabling low-voltage capacitors to be used to reduce the system cost and volume.
2. The inrush current is suppressed and the traditional topology can be started off with a soft start capability.
3. Control of the speed of the induction motor, thus providing with a constant speed application that can be used in various forms.

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